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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Yuji YAGI et al.

Serial No.: 09/754,133

Filed: January 5, 2001

For: CIRCUIT BOARD AND SEMICONDUCTOR DEVICE, AND METHOD OF MANUFACTURING THE SAME

On Appeal from:

Group Art Unit: 3729

Examiner: Rick Kiltae Chang

BRIEF ON APPEAL

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I. REAL PARTY IN INTEREST

The real party in interest is Matsushita Electric Industrial Co., Ltd. of Osaka, Japan, whose ownership interest is shown in an assignment recorded August 9, 1999 at Reel 10151, Frame 0318.

II. RELATED APPEALS AND INTERFERENCES

There is no appeal or interference known to appellants, the assignee or the undersigned that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

The application is a divisional application under 37 C.F.R. §1.53(b) of application Serial Number 09/332,968, filed June 15, 1999. Claims 1 to 23 were canceled upon filing the present application (those claims were examined in the parent case) and claims 24 to 34 were presented for examination here. Claims 24, 26, 29 and 31 were revised in an Amendment Under 37 CFR 1.111 filed April 8, 2002. Claims 24 to 26 and 29 to 31 were further revised in an Amendment Under 37 CFR 1.116 filed October 7, 2002; that paper was entered when a 37 CFR 1.114 Request for Continued

Examination (RCE) was filed November 8, 2002. Claims 24 and 29 were revised and new claims 35 and 36 were added in an Amendment Under 37 CFR 1.111 filed April 30, 2003. Claims 26 to 28 and 31 to 34 stand withdrawn as directed to non-elected species. Claims 24, 25, 29, 30, 35 and 36 are on appeal.

IV. STATUS OF AMENDMENTS

An appeal was taken directly from the Final Rejection. Thus, no amendment is awaiting or has been denied entry. The claims on appeal in the Appendix correspond to the claims that were finally rejected.

V. SUMMARY OF INVENTION

The invention set out in the claims on appeal is directed to a method of simultaneously and unitarily forming wiring patterns and protrusions on a surface of a substrate.

The limitation "simultaneously and unitarily" (recited in both independent claims 24 and 29) in the context of the claims means forming at one time both wiring patterns and protrusions as a unitized, contiguous single unit.

A major and apparent objective of the claimed invention is to be able to reduce the time required to manufacture a circuit board having a wiring pattern and structures called "protrusions" for mounting a semiconductor device thereon, and at the same time, to make such protrusions with identical shapes and heights; see the specification at page 1, line 31, to page 2, line 10; page 2, lines 14 to 18; page 3, lines 3 to 11; page 8, lines 21 to 30; page 12, lines 22 to 31; the paragraph bridging pages 13 and 14; and page 15, lines 18 to 23.

Both independent claims (24 and 29) are directed to methods for simultaneously and unitarily forming wiring patterns and protrusions on a surface of a substrate. All remaining claims on appeal depend directly or indirectly from claim 24 or claim 29.

VI. ISSUES

The issues before the Board are

(1) whether the subject matter of claims 24, 25 and 35 patentably defines over (35 USC 102) the teachings of Abe (U.S. Patent 5,746,868);

(2) whether the subject matter of claims 29 to 30 patentably defines over (35 USC 103) the teachings of Abe '868 in view of Official Notice; and

(3) whether the subject matter of claim 36 patentably defines over (35 USC 103) the teachings of Abe '868 taken with Murakami (U.S. Patent 5,874,780).

VII. GROUPING OF CLAIMS

For purposes of appeal, claims 24, 25, 29, 30, 35 and 36 each stand or fall independently of each other. The claims represent separate embodiments of the invention. It is noted that no present art rejection address all claims. Thus, the claims do not stand or fall together.

VIII. ARGUMENT

1. Summary of Argument

One of ordinary skill in the art is not directed to the claimed invention from a consideration of either Abe '868 alone or a collective consideration of all the cited references. The claims all contain a process treatment feature (simultaneously and unitarily forming wiring patterns and protrusions on a surface of a

substrate) that is neither shown in nor suggested by the cited art. Claims 29 and 35 also call for such protrusions to have substantially equal heights, and claims 25 and 30 also call for the protrusions and wiring patterns to be made of the same conductive sintered material. Such features are not taught or suggested by the cited art.

2. Abe '868

The Examiner has asserted that Abe '868 discloses a method for simultaneously and unitarily forming wiring patterns and protrusions on a surface of a substrate in the same manner as claimed herein. The Examiner alleges that Abe '868, Figs. 1A-1E, discloses simultaneously and unitarily forming element 9 with protrusions and wiring patterns. See the second paragraph of section 2 on page 2 of the Office Action (Final Rejection) mailed July 8, 2003 (which repeats an identical rejection from the Office Action mailed February 26, 2003). In section 6 of the July 8 Office Action (see page 3), the Examiner states that

> [f]ig. 1D shows the unitary and simultaneously forming step in the hole formed in Fig. 1C. Examiner is only interested in the formation as shown in Fig. 1D, not other extraneous steps as they are noted by the applicants.

Appellants have explained before Abe '868, Figs. 1A-1E (including Fig. 1D), do not show the claimed method.

In Abe '868, interconnection 2 (allegedly corresponding to appellants' "wiring pattern") is formed in an initial step (Fig. 1A), while interconnection 9 (allegedly corresponding to appellants' "protrusion") is not formed or made unitary with interconnection 2 until almost the very end of the manufacturing sequence, i.e., when conductive paste 7 is located on top of interconnection 2 in Fig. 1D, followed by a sintering step that makes interconnection 9 unitary with interconnection 2 in Fig. 1E. Accordingly, because the wiring pattern/interconnection 2 is formed at an initial step shown in Fig. 1A and protrusion/interconnection 9 is formed at a final step shown in Fig. 1E, necessarily, Abe '868 does not disclose a method of simultaneously and unitarily forming wiring patterns and protrusions on a surface of a substrate. The reference drawings simply don't show what appellants claim.

More detailedly, Abe '868, Fig. 1A, shows interconnection element 2 located on substrate 1, and column 5, lines 8-9, describes Fig. 1A as showing interconnection 2 in a first layer formed on substrate 1. Figs. 1B-C show intervening steps wherein insulating and protective films are formed on interconnection 2 to

form surfaces in preparation for a future step of applying an additional metal conductor. Fig. 1D shows conductive paste 7 applied to hole 5 above interconnection 2. This step differs completely from step 1A and forms a layer different than the "first layer" formed in step 1A. And finally, Fig. 1E shows interconnection 9 formed on top of interconnection 2 after the paste is sintered and the protective film has been removed, as described at column 5, beginning at line 65. Fig. 1E is separated from initial Step 1A by the intervening steps of Figs. 1B-1D; while Fig. 1E shows a unitary formation of interconnections 2 and 9 as a unitized structure, Abe '868 does not describe the method step of simultaneously "and" unitarily forming interconnections 2 and 9 to form the structure shown in Fig. 1E, because interconnection 9 is not made unitary with interconnection 2 until almost the very end of the manufacturing sequence, i.e., at a sintering substep of the last step 1E. Therefore, contrary to the statement in the Final Rejection, Abe '868 does not disclose the step of simultaneously "and" unitarily forming wiring patterns and protrusions, because steps 1A and 1E are not simultaneous in time, as required by the claims on appeal.

3. Official Notice

The Examiner takes Official Notice "that it is well known in the art to coupling [SIC] electrically the protrusion with a semiconductor chip component to form a motherboard"; see the last sentence on page 2 of the Final Rejection. The Examiner asserts that the subject matter of claims 29 and 30 would have been obvious from a joint consideration of Abe '868 and the indicated Official Notice.

The deficiencies of Abe '868 have been detailed above. The Official Notice overcomes none of those deficiencies. Claims 29 and 30 are patentable also.

4. Murakami '780

The invention in the claims on appeal is directed to a method of simultaneously and unitarily forming wiring patterns and protrusions on a surface of a substrate, and further calls for modifying the protrusions to have substantially equal heights by imposing a load on the protrusions.

Murakami '780 has been cited to show a technique involving imposing a load on a bump electrode of a semiconductor device. The Examiner asserts that it would have been obvious to use such a

teaching in combination with Abe '868 because of the importance of achieving better alignment and adherence with the mounting device. The Examiner concludes that it would have been obvious to the artisan at the time of the instant invention to modify the method of Abe '868 to include the load imposing method taught by Murakami '780. Nevertheless, Abe '868 does not disclose the presently claimed invention as described in the independent claims for the reasons discussed herein, and Murakami '780 does not overcome those indicated deficiencies.

5. The Purported Justification of the Rejection

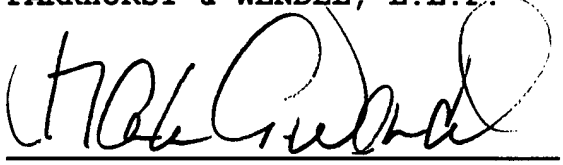
The Examiner at 6. on page 3 of the Final Rejection purports to justify the rejections based upon Abe '868 by remarking that "Fig. 1D [of the patent] shows the unitary and simultaneously forming step in the hole formed in Fig. 1C." He states also that he "is only interested in the formation as shown in Fig. 1D [of the reference], not other extraneous steps as they are noted by the applicants." As explained above, the Examiner's analysis and interpretation of Abe '868 are wrong. One cannot focus only on the Fig. 1D step of the reference. The rejection and the justification therefore are both improper.

IX. CONCLUSION

For the foregoing reasons, it is respectfully submitted that claims 24, 25, 29, 30, 35 and 36 patentably define over the cited references and the Board is requested to so rule.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.



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